CLAIMS

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a plurality of first memory cells arranged in matrix;

a control line connecting a subset of the plurality of first memory cells which are aligned in a row direction or a column direction; and

a second memory cell connected to the control line,

wherein the second memory cell is configured to retain information on a stress applied from the control line to each of the first memory cells.

2. A semiconductor memory device comprising:

a plurality of first memory cells arranged in matrix;

a plurality of word lines each connecting a subset of the plurality of first memory cells which are aligned in a row direction;

a plurality of bit lines each connecting a subset of the plurality of first memory cells which are aligned in a column direction; and

a plurality of second memory cells which are connected to at least either of the word lines and the bit lines,

wherein the first memory cells and the second memory cells each have a charge storage portion for storing charges, and

when voltage application to the word lines or the bit lines changes the amounts of charges stored in the charge storage portions of the first memory cells and the second memory cells, the amount of change in charges in the second memory cell is larger than the amount of change in charges in the first memory cell.

3. The device of claim 2,

wherein the first memory cells and the second memory cells each have a floating gate electrode which is formed, as the charge storage portion, above a semiconductor

substrate with a tunnel insulating film interposed therebetween, a control gate electrode formed above the floating gate electrode with a capacitor insulating film interposed therebetween, and a source electrode and a drain electrode provided to interpose a portion of the semiconductor substrate located below the floating gate electrode, and

the first memory cells differ from the second memory cells in the composition or the shape of at least one of the tunnel insulating film, the floating gate electrode, the capacitor insulating film, and the control gate electrode.

4. The device of claim 3, wherein the capacitor insulating films of the second memory cells have a lower resistivity than the capacitor insulating films of the first memory cells.

5. The device of claim 4, wherein the capacitor insulating films of the first memory cells are each formed as a stacked film containing a silicon oxide film and a silicon nitride film, and the capacitor insulating films of the second memory cells are each formed as a single layer film or a stacked film containing a silicon oxide film.

6. The device of claim 3, wherein the floating gate electrodes of the first memory cells are each formed to have a smooth upper surface, and the floating gate electrodes of the second memory cells are each formed to have an upper surface with projections and depressions.

7. The device of claim 3, wherein in terms of the ratio of the area in which the floating gate electrode and the control gate electrode face each other with the capacitor insulating film interposed therebetween to the area in which the semiconductor substrate and the floating gate electrode face each other with the tunnel insulating film interposed therebetween, the second memory cells are larger than the first memory cells.

8. The device of claim 2, further comprising switch means for separating electrical connections between the word lines or the bit lines and the second memory cells.

9. The device of claim 8, wherein the switch means is a fuse element.

10. The device of claim 8, wherein the switch means is a MIS transistor.

11. The device of claim 10, wherein at least one of the first memory cells stores control information with which turn-on or turn-off of the MIS transistor is controlled.

12. The device of claim 2, wherein the plurality of second memory cells are arranged with two or more being connected in serial on each of the word and/or bit lines.

13. The device of claim 12, further comprising an equalization circuit for equalizing pieces of data stored in the second memory cells connected in serial and supplying the equalization result.

14. The device of claim 2, wherein the plurality of second memory cells are arranged with two or more being connected in parallel on each of the word and/or bit lines.

15. The device of claim 14, further comprising switch transistors for controlling connections between the second memory cells and at least either of the word lines and the bit lines.

16. The device of claim 2, further comprising:

a first verification circuit for determining whether or not a writing operation or an erasing operation is normally performed on the first memory cells; and

a second verification circuit for determining whether or not a writing operation or an erasing operation is normally performed on the second memory cells.

17. The device of claim 16, wherein the first memory cells and the second memory cells are formed of the same members.

18. The device of claim 2, further comprising:

a first source line connected to source electrodes of the first memory cells; and

a second source line connected to source electrodes of the second memory cells.

19. The device of claim 18, wherein the first memory cells and the second memory cells are formed of the same members.

20. The device of claim 2,

wherein the plurality of second memory cells are arranged with two or more being connected in serial on each of the word and/or bit lines, and

the second memory cells connected in serial includes an identically-shaped cell formed of the same members as the first memory cells and a differently-shaped cell formed of different members from the first memory cells.